Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A circuit comprising:

a first phase-locked loop ~~(PLL)~~ to receive a first reference signal and a first feedback signal, and to produce a data clock signal having a first frequency based at least in part upon ~~differences between~~ the first reference signal and a first feedback signal; and

a second phase-locked loop ~~PLL~~ coupled to the first ~~PLL~~ phase-locked loop by a first signal path, the second phase-locked loop to receive a second reference signal on the first signal path and a second feedback signal on a second signal path~~,~~ and to produce a second clock signal having a second frequency based at least in part upon ~~differences between~~ the second reference signal and the second feedback signal, the first feedback signal and the second reference signal being derived from the data clock signal and the second feedback signal being derived from the second clock signal, wherein the second reference signal and the second feedback signal have equivalent signal distribution delays.

2. (currently amended) The circuit of claim 1, further comprising a first divide-by-N circuit coupled to the first ~~PLL~~ phase-locked loop circuit to divide the first frequency of the data clock signal by a first integer value N to produce the first feedback signal having a third frequency.

3. (currently amended) The circuit of claim 2, further comprising a divide-by-M circuit coupled between the first ~~PLL~~ phase-locked loop circuit and the second ~~PLL~~ phase-locked loop circuit to divide the first frequency of the data clock signal by an integer value M to produce the second reference signal.

4. (original) The circuit of claim 3, wherein the divide-by-M circuit is equipped to divide the first frequency of the data clock signal by a selected one of a factor of 4, 2 and 1.

5. (original) The circuit of claim 4, wherein the first divide-by-N circuit comprises a divide-by-4 circuit to divide the first frequency of the data clock signal by a factor of 4.

6. (currently amended) The circuit of claim 3, further comprising a second divide-by-N circuit coupled to the second ~~PLL~~ phase-locked loop to divide the second frequency of the second clock signal by a second integer value N to produce the second feedback signal, wherein the second integer value N is selected from a group of integer values including a low integer value, and a high integer value that is less than two times the low integer value.

7. (canceled)

8. (currently amended) The circuit of claim 1, whereinfurther comprising:

the a first signal path corresponding to the second reference signal; and

the a second signal path corresponding to the second feedback signal, wherein the first and second signal paths are equivalent in length.

9. (currently amended) A microprocessor processor comprising:

a processoring core;

I/O input-output circuitry; and

a clock generation circuit comprising:

a first phase-locked loop (PLL) circuit coupled to the input-output circuitry by a first signal trace, the first phase-locked loop to produce producing a first output signal having a first frequency based at least in part upon a first reference signal and a first feedback signal derived from the first output signal, and providing the first output signal to be used as a data clock signal for to the I/O input-output circuitry on the first signal trace; and

a second ~~PLL circuit~~ phase-locked loop coupled to the first ~~PLL~~ phase-locked loop by a second signal trace and to the processor core circuitry by a third signal trace, the second phase-locked loop ~~to produce~~ providing a second output clock signal to the processor core circuitry on the third signal trace, the second output signal having a second frequency based at least in part upon a second reference signal provided by the second signal trace and derived from the first output signal and a second feedback signal derived from the second output signal~~, the second output signal to be used as a clock signal for the processor core~~.

10. (currently amended) The ~~micro~~processor of claim 9, further comprising a first divide-by-N circuit coupled to the first ~~PLL circuit~~ phase-locked loop to divide the first frequency of the data clock signal by a first integer value N to produce the first feedback signal having a third frequency.

11. (currently amended) The ~~micro~~processor of claim 10, further comprising a divide-by-M circuit coupled between the first ~~PLL circuit~~Phase-locked loop and the second ~~PLL circuit~~Phase-locked loop to divide the first frequency of the data clock signal by an integer value M to produce the second reference signal.

12. (currently amended) The ~~circuit~~ processor of claim 11, wherein the divide-by-M circuit is equipped to divide the first frequency of the data clock signal by a selected one of a factor of 4, 2 and 1.

13. (currently amended) The ~~circuit~~ processor of claim 12, wherein the first divide-by-N circuit comprises a divide-by-4 circuit to divide the first frequency of the data clock signal by a factor of 4.

14. (currently amended) The ~~circuit~~ processor of claim 11, further comprising a second divide-by-N circuit coupled to the second ~~PLL~~ phase-locked loop to divide the second frequency of the core clock signal by a second integer value N to produce the second feedback signal, wherein the second integer value N is selected from a group of integer values including a low integer value and a high integer value that is less than two times the low integer value.

15. (canceled)

16. (currently amended) The ~~circuit~~ processor of claim 9, further comprising:

~~a first signal path corresponding to the second reference signal; and~~

a ~~second~~ fourth signal trace ~~path corresponding~~ to provide the second feedback signal, wherein the ~~first and~~ second and fourth signal traces~~paths~~ have equivalent signal distribution delays~~are equivalent in length~~.

17-19. (canceled)

20. (new) The processor of claim 16, wherein the second and fourth signal traces are equivalent in length.

Amendments to the Drawings

The attached sheet of drawings includes changes to Fig. 1. This sheet replaces the original sheet including Fig. 1. Figure 1 has been amended to include a "Prior Art" label.